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(Benchmark Code) Rev 1.0 Apr 2019: Voted Best Paper 1st Place: DVCON 2016 Using UVM Virtual Sequencers & Virtual Sequences Rev 1.1 Sep 2019 : DVCON 2011 OVM & UVM Techniques for Terminating Tests Rev 1.1 Mar 2011 : DVCON 2003 The IEEE Verilog-2001 Simulation Tool Scoreboard Rev 1.2 Apr 2003 : HDLCON 2002

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GitHub - riscv/riscv-cores-list: RISC-V Cores, SoC ...

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Code refactoring - Wikipedia

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Getting Started with Zynq - Digilent Reference

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